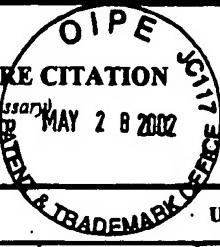


## INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

MAY 28 2002



Docket Number (Optional)

BUR920010192US1

Application Number

10/063427

Applicant(s)

Mitchell DeHond, et al.

Filing Date

04/23/02

Group Art Unit

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
BB		3,751,647	08/07/73	Maeder, et al.			
BB		5,084,824	01/28/92	Lam, et al.			
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## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
BB		JP6216249	08/05/94	Japan				
BB		JP1024225	09/11/98	Japan				

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

BB		Michael Rettersdorf, "Yield Focused Defect Reduction Methodology", 3/99, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 309 - 313
BB		K.W. Lallier and A.D. Savkar, "Relating Logic Design to Physical Geometry in LSI Chip", IBM Technical Disclosure Bulletin, Vol. 19 No. 6, November 1976, pp. 2140-2143.

EXAMINER

DATE CONSIDERED

3/5/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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